

Customer No.: 31561
Application No.: 10/710,672
Docket No.: 13039-US-PA

AMENDMENT

To the Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

Claims 1-2 (cancelled)

Claim 3. (withdrawn) The method of claim 2, wherein the charge storage material layer is a silicon nitride layer or a silicon oxynitride layer.

Claims 4-10. (cancelled)

Claim 11. (currently amended) A method of fabricating a dual bit flash memory, comprising the steps of:

providing a substrate;

forming a tunneling dielectric layer over the substrate;

forming a patterned mask layer over the tunneling dielectric layer, wherein the patterned mask layer has a trench;

forming a conductive layer over the substrate to cover the surface of the trench;

removing a portion of the conductive layer to form a pair of conductive spacers on the respective sidewalls of the trench to serve as floating gates;

removing the patterned mask layer;

forming an inter-gate dielectric layer over the substrate to cover the floating gates and the tunneling dielectric layer;

forming a control gate over the inter-gate dielectric layer above the conductive

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spacers;

forming a pair of dielectric spacers on the sidewalls of the control gate;

removing portions of the inter-gate dielectric layer and the tunneling dielectric layer by using the dielectric spacers and the control gate as hard masks; and

forming source/drain regions in the substrate on each side of the control gate.

Claim 12. (original) The method of claim 11, wherein the tunneling dielectric layer comprises a silicon oxide layer.

Claim 13. (original) The method of claim 11, wherein the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer.

Claim 14. (original) The method of claim 11, wherein the inter-gate dielectric layer is an oxide-nitride-oxide composite layer, an oxide-nitride layer or a silicon oxide layer.

Claim 15. (original) The method of claim 11, wherein the conductive layer comprises a doped polysilicon layer.

Claim 16. (original) The method of claim 13, wherein the step of removing the patterned mask layer comprises performing a wet etching operation using hot phosphoric acid solution.

Claim 17. (cancelled)

Claim 18. (withdrawn) A method of fabricating a silicon-oxide-nitride-oxide-silicon (SONOS) memory, comprising the steps of:

providing a substrate;

forming a bottom silicon oxide layer over the substrate;

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forming a patterned mask layer over the bottom silicon oxide layer, wherein the patterned mask layer has a trench;

forming a charge-trapping layer over the substrate to cover the surface of the trench;

removing a portion of the charge-trapping layer to form a pair of charge storage spacers on the sidewalls of the trench;

removing the patterned mask layer;

forming a top silicon oxide layer over the substrate to cover the pair of charge storage spacers and the bottom silicon oxide layer;

forming a gate over the top silicon oxide layer above the pair of charge storage spacers; and

forming source/drain regions in the substrate on each side of the gate.

Claim 19. (withdrawn) The method of claim 18, wherein the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer.

Claim 20. (withdrawn) The method of claim 18, wherein the charge-trapping layer is a silicon nitride layer or a silicon oxynitride layer.

Claim 21. (withdrawn) The method of claim 18, wherein after forming the gate over the top silicon oxide layer, further comprises:

forming a pair of dielectric spacers on the sidewalls of the gate but exposing the top silicon oxide layer; and

removing portions of the top silicon oxide layer and the underlying tunneling dielectric layer by using the dielectric spacers and the gate as hard masks.